Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Balance**
2. **Input –**
3. **Input +**
4. **V –**
5. **Balance**
6. **Output**
7. **V +**

**.042”**

**.073”**

**2 1 7**

**3 4 5 6**

**1**

**5**

**6**

**A**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si or Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 156 A**

**APPROVED BY: DK DIE SIZE .042” X .073” DATE: 8/30/21**

**MFG: NATIONAL THICKNESS .014” P/N: LF355**

**DG 10.1.2**

#### Rev B, 7/19/02